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EXAMINER	
KANG, SUK JIN	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/614,519	DUBOIS, MICHEL	
	Examiner	Art Unit	
	Suk Jin Kang	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged.

Information Disclosure Statement

2. The information disclosure statement submitted on December 22, 2003 has been considered by the Examiner and made of record in the application.

Specification

3. The abstract of the disclosure is objected to because it should be limited to a single paragraph within a range of 50 to 150 words and/or 15 lines of text. Correction is required. See MPEP § 608.01(b).

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. **Claim 10** is objected to because of the following informalities:

a) On **line 2** of **claim 10**, replace "have" with --has-- after "that".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 33-34** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 33 refers to steps of claim 8, which states, "The system of claims 5 or 6 wherein the memory comprises Read Only Memory." Because claim 8, in its present form, does not include steps in regard to applicant's claimed invention, the Examiner feels it is impossible to determine the scope of the claim. Upon clarification, and/or amending the above claim, the Examiner will be able to properly act on the merits of this claim. It should also be noted, that no new matter be incorporated.

8. **Claim 34** is rejected under 35 U.S.C. 112, second paragraph, because its failure to resolve the deficiency of Claim 33. Upon clarification, and/or amending the above claim, the Examiner will be able to properly act on the merits of this claim. It should also be noted, that no new matter be incorporated.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 1, 2, 4, 5-10, and 18-26** are rejected under 35 U.S.C. 102(e) as being anticipated by **Argentati (U.S. Patent # 5,754,120)**.

Consider **claim 1**, Argentati discloses a digital cross connect system, comprising: a switch matrix subsystem comprising a plurality of switch matrix units in a CLOS arrangement in multiple stages (abstract, figure 1-6, column 4 lines 28-40), each switch matrix unit having a plurality of input ports and output ports (figure 2, column 5 lines 33-55), at least two of the switch matrix units having a number of their output ports uniquely connected to input ports on one of the switch matrix units in the next stage (figure 2, column 5 lines 33-55) and having an equal number of their output ports uniquely connected to input ports on another of the switch matrix units in the next stage (figure 2, column 5 lines 33-55); a plurality of subsystem input ports associated with the switch matrix subsystem (figure 1-6, column 4 lines 28-40, column 5 lines 33-55); a plurality of subsystem output ports associated with the switch matrix subsystem (figure 1-6, column 4 lines 28-40, column 5 lines 33-55); and switch matrix unit programming that instructs the switch matrix units to generate specific internal cross-connections that allow one or more input signals present at one or more subsystem input ports to be connected to one or more subsystem output ports (controller subsystem, figure 1, column 4 lines 41-53, column 6 lines 6-18).

Consider **claim 2**, and **as applied to claim 1 above**, Argentati discloses the system wherein the switch matrix subsystem comprises a three-stage architecture having at least two switch matrix units in each stage (abstract, figure 1-6, column 4 lines 28-40).

Consider **claim 4**, and **as applied to claim 1 above**, Argentati discloses the system wherein the switch matrix unit programming is generated by a method with steps comprising: obtaining information that identifies a specific subsystem input port and a desired subsystem output port for connecting to the specific subsystem input port (column 3 lines 7-22, column 6 lines 6-18); identifying a pathway from a switch matrix unit in the cross connect system that provides the specific subsystem input port to a switch matrix unit in the cross connect system that provides the desired subsystem output port (column 9 lines 58-94, column 10 lines 51-59); determining that sufficient channels exist in the identified pathway to allow a connection from the specific subsystem input port to the desired subsystem output port (figure 8, column 10 lines 28-59); identifying specific channels in the identified pathway to allow a connection from the specific subsystem input port to the desired subsystem output port (figure 8, column 10 lines 51-59); and storing in a programming data structure information identifying connections that have to be made in a plurality of switch matrix units in the cross connect system to allow the connection from the specific subsystem input port to the desired subsystem output port (107-108, figure 8, column 10 lines 60-67, column 11 lines 1-7).

Consider **claim 5**, and **as applied to claim 1 above**, Argentati discloses the system wherein the programming comprises instructions stored in memory (figure 1, column 4 lines 54-67, column 5 lines 1-15).

Consider **claim 6**, and **as applied to claim 1 above**, Argentati discloses the system wherein the programming comprises an arrangement of binary values stored in memory (figure 3-6, ICM, OCM, column 6 lines 6-50).

Consider **claim 7**, and **as applied to claim 1 above**, Argentati discloses the system wherein the programming comprises software code stored in memory (column 4 lines 54-65).

Consider **claim 8**, and **as applied to claim 5 or 6 above**, Argentati discloses the system wherein the memory comprises Read Only Memory (column 4 lines 60-65).

Consider **claim 9**, and **as applied to claim 5 or 6 above**, Argentati discloses the system wherein the memory comprises Random Access Memory (28, figure 1, column 4 lines 54-67, column 5 lines 1-15).

Consider **claim 10**, and **as applied to claim 1 above**, Argentati discloses the system wherein the programming comprises a programmable circuit element that has been programmed (14, figure 1, column 4 lines 41-65).

Consider **claim 18**, Argentati discloses a method for generating switch matrix unit programming for switch matrix units of a cross connect device, comprising: obtaining information that identifies an input port of the cross connect device and a desired output port of the cross connect device for connecting to the identified input port (column 3 lines 7-22, column 6 lines 6-18); identifying a pathway from a switch matrix unit in the cross connect device that provides the identified input port to a switch matrix unit in the cross connect device that provides the desired output port (column 9 lines 58-94, column 10 lines 51-59); determining that sufficient channels exist in the identified

pathway to allow a connection from the identified input port to the desired output port (figure 8, column 10 lines 28-59); identifying specific channels in the identified pathway to allow a connection from the identified input port to the desired output port (figure 8, column 10 lines 51-59); and storing in a programming data structure information identifying connections that have to be made in a plurality of switch matrix units in the cross connect device to allow the connection from the identified input port to the desired output port (107-108, figure 8, column 10 lines 60-67, column 11 lines 1-7).

Consider **claim 19**, and **as applied to claim 18 above**, Argentati discloses the method further comprising using the programming data structure to generate the switch matrix unit programming for switch matrix units of the cross connect device, the switch matrix unit programming identifying internal connections that have to be made within the switch matrix units to connect the identified input to the desired output (controller subsystem, figure 1, column 4 lines 41-53, column 6 lines 6-18).

Consider **claims 20 and 22**, and **as applied to claim 18 above**, Argentati discloses the method wherein the step of identifying a pathway comprises identifying a preferred pathway instead of an alternate pathway and identifying an alternate pathway instead of a preferred pathway (path matrix, figure 3-6, column 3 lines 7-30, column 10 lines 60-67, column 11 lines 1-7).

Consider **claims 21 and 23**, and **as applied to claims 20 and 22 above**, respectively, Argentati discloses the method wherein the step of identifying a preferred pathway comprises identifying the preferred pathway when the alternate pathway was identified in a prior iteration and the alternate pathway when the preferred pathway was

identified in a prior iteration (107-108, figure 8, column 3 lines 7-30, column 10 lines 60-67, column 11 lines 1-7 and 16-40).

Consider **claim 24, and as applied to claim 18 above**, Argentati discloses the method wherein the step of determining that sufficient channels exist comprises: remembering the number of available output ports for a plurality of the switch matrix units; and determining that each switch matrix unit that has output ports in the identified pathway has an available output port (OCM, figure 3-6, column 6 lines 35-38, column 10 lines 60-67, column 11 lines 1-7).

Consider **claim 25**, and **as applied to claim 24 above**, Argentati discloses the method wherein the remembering step comprises keeping a count of the number of output ports that are not available (OCM, column 6 lines 6-59, column 8 lines 18-28).

Consider **claim 26**, and **as applied to claim 25 above**, Argentati discloses the method wherein the step of identifying specific channels comprises incrementing the count of output ports that are not available (column 10 lines 60-67, column 11 lines 1-7).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. **Claims 3, 16, 17, 35, and 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Argentati (U.S. Patent # 5,754,120)** in view of **Taylor (U.S. Patent # 5,313,590)**.

Consider **claim 3**, and **as applied to claim 2 above**, Argentati discloses the system wherein the inputs ports of the first stage switch matrix units are inputs ports for the switch matrix subsystem (figure 1-6, column 4 lines 28-40, column 5 lines 33-55) and the output ports of the third stage switch matrix units are output ports for the switch matrix subsystem (figure 1-6, column 4 lines 28-40, column 5 lines 33-55), but does not expressly disclose each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage.

In the same field of endeavor, Taylor discloses each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output

set B associated with that switch matrix unit (figure 2A, figure 3, column 4 lines 52-63, column 7 lines 26-45), each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage (figure 2A, figure 3, column 7 lines 26-54).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the output sets as taught by Taylor with the system as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 16**, Argentati discloses an apparatus that performs a switching function, comprising: a plurality of switch matrix units each having input ports and output ports (figure 2, column 5 lines 33-55), at least six of said switch matrix units are organized in three stages with two switch matrix units in each stage (figure 2-6, column 5 lines 32-55), the inputs ports of the first stage switch matrix units being inputs ports for the apparatus and the output ports of the third stage switch matrix units being output ports for the apparatus (figure 1-6, column 4 lines 28-40, column 5 lines 33-55); each switch matrix unit being programmable to provide connections between its input ports and its output ports (controller subsystem, figure 1, column 4 lines 41-53, column 6 lines 6-18); and switch matrix unit programming for each first stage, second stage and third stage switch matrix units, the programming instructing at least one of the first stage switch matrix units, at least one of the second stage switch matrix units and at least one

of the third stage switch matrix units to each establish an internal connection that allows a signal appearing at one of the inputs of the apparatus to be switched to at least one of the outputs of the apparatus (107-108, figure 8, column 10 lines 60-67, column 11 lines 1-7), but does not expressly disclose each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage.

In the same field of endeavor, Taylor discloses each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit (figure 2A, figure 3, column 4 lines 52-63, column 7 lines 26-45), each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage (figure 2A, figure 3, column 7 lines 26-54).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the output sets as taught by Taylor with the system as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 17**, and **as applied to claim 16 above**, Argentati, as modified by Taylor, discloses the apparatus wherein the programming is generated using a method with steps comprising: obtaining information that identifies an input port of the apparatus and a desired output port of the apparatus for connecting to the identified input port (column 3 lines 7-22, column 6 lines 6-18); identifying a pathway from a switch matrix unit in the apparatus that provides the identified input port to a switch matrix unit in the apparatus that provides the desired output port (column 9 lines 58-94, column 10 lines 51-59); determining that sufficient channels exist in the identified pathway to allow a connection from the identified input port to the desired output port (figure 8, column 10 lines 28-59); identifying specific channels in the identified pathway to allow a connection from the identified input port to the desired output port (figure 8, column 10 lines 51-59); and storing in a programming data structure information identifying connections that have to be made in a plurality of switch matrix units in the apparatus to allow the connection from the identified input port to the desired output port (107-108, figure 8, column 10 lines 60-67, column 11 lines 1-7).

Consider **claim 35**, Argentati discloses a method for programming an apparatus having at least six switch matrix units wherein the six switch matrix units are organized in three stages with two switch matrix units in each stage (figure 2-6, column 5 lines 32-55), the inputs ports of the first stage switch matrix units being inputs ports for the apparatus and the output ports of the third stage switch matrix units being output ports for the apparatus (figure 1-6, column 4 lines 28-40, column 5 lines 33-55), each switch matrix unit being programmable to provide connections between its input ports and its

output ports (controller subsystem, figure 1, column 4 lines 41-53, column 6 lines 6-18), the method comprising: calculating a path for a signal on an input port for the apparatus to an output port for the apparatus (column 9 lines 58-94, column 10 lines 51-59); and programming at least one of the first stage switch matrix units, at least one of the second stage switch matrix units and at least one of the third stage switch matrix units to each establish an internal connection that allows a signal appearing at the input port for the apparatus to be connected to an output port for the apparatus (107-108, figure 8, column 3 lines 7-22, column 6 lines 6-18, column 10 lines 60-67, column 11 lines 1-7), but does not expressly disclose each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage.

In the same field of endeavor, Taylor discloses each first stage and second stage switch matrix unit having its output ports assigned to either an output set A or an output set B associated with that switch matrix unit, each output port in output set A of a switch matrix unit being uniquely coupled to an input port in one of the two switch matrix units in the next stage and each output port in output set B of a switch matrix unit being uniquely coupled to an input port in the other of the two switch matrix units in the next stage.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the output sets as taught by Taylor with the system as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 36**, and **as applied to claim 35 above**, Argentati, as modified by Taylor, discloses the method wherein the calculating step comprises identifying a pathway from a switch matrix unit in the apparatus that provides the input port to the switch matrix unit in the apparatus that provides the desired output port (column 9 lines 58-94, column 10 lines 51-59); determining that sufficient channels exist in the identified pathway to allow a connection from the identified input port to the desired output port (figure 8, column 10 lines 28-59); and identifying specific channels in the identified pathway to allow a connection from the identified input port to the desired output port (figure 8, column 10 lines 51-59).

13. **Claims 11-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Argentati (U.S. Patent # 5,754,120)** in view of **Anderson et al. (U.S. Patent # 4,821,034)**.

Consider **claims 11 and 12**, and **as applied to claim 10 above**, Argentati discloses the claimed invention, but does not expressly disclose the system wherein the programmable circuit element comprises an application specific integrated circuit and a programmable logic array.

In the same field of endeavor, Anderson et al. disclose the system wherein the programmable circuit element comprises an application specific integrated circuit (column 26 lines 32-44) and a programmable logic array (column 22 lines 55-67, column 23 lines 1-11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the ASIC and programmable logic array as taught by Anderson et al. with the system as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claims 13 and 14**, and **as applied to claim 1 above**, Argentati discloses the claimed invention, but does not expressly disclose the system wherein each switch matrix unit comprises an application specific integrated circuit and a square matrix.

In the same field of endeavor, Anderson et al. disclose the system wherein each switch matrix unit comprises an application specific integrated circuit (column 26 lines 32-44) and a square matrix (figure 3, column 5 lines 51-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate ASIC and square matrix as taught by Anderson et al. with the system as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 15**, and **as applied to claim 1 above**, Argentati discloses the claimed invention, but does not expressly disclose the system wherein the number of input ports for each switch matrix unit is the same.

In the same field of endeavor, Anderson et al. disclose the system wherein the number of input ports for each switch matrix unit is the same (figure 3, column 5 lines 51-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the same number of input ports for each switch matrix as taught by Anderson et al. with the system as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

14. **Claims 27-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Argentati (U.S. Patent # 5,754,120)** in view of **Yoshifuji (U.S. Patent # 5,450,074)**.

Consider **claim 27**, and **as applied to claim 18 above**, Argentati discloses the claimed invention, but does not expressly disclose the method wherein the step of identifying specific channels comprises: identifying specific output ports in specific switch matrix units that are in the identified pathway that are available; and reserving the identified specific output ports for use in making the connection from the identified input port to the desired output port.

In the same field of endeavor, Yoshifuji discloses the method wherein the step of identifying specific channels comprises: identifying specific output ports in specific switch matrix units that are in the identified pathway that are available (figure 4, column 4 lines 42-67, column 5 lines 1-31); and reserving the identified specific output ports for use in making the connection from the identified input port to the desired output port (figure 3-4, column 4 lines 42-67, column 5 lines 1-31).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the identifying and reserving of specific output ports as taught by Yoshifuji with the method as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 28**, and **as applied to claim 27 above**, Argentati discloses the claimed invention, but does not expressly disclose the method wherein the step of identifying specific output ports comprises: assigning a numerical value to the output ports; and identifying available output ports that have the lowest numerical value.

In the same field of endeavor, Yoshifuji discloses the method wherein the step of identifying specific output ports comprises: assigning a numerical value to the output ports; and identifying available output ports that have the lowest numerical value (figure 3-8, column 5 lines 20-67, column 6 lines 1-31).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate assigning a numerical value to the output port as taught by Yoshifuji with the method as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 29**, and **as applied to claim 18 above**, Argentati discloses the claimed invention, but does not expressly disclose the method wherein the step of obtaining information that identifies an input port comprises obtaining information that identifies a plurality of input port and desired output port pairs.

In the same field of endeavor, Yoshifuji discloses the method wherein the step of obtaining information that identifies an input port comprises obtaining information that

identifies a plurality of input port and desired output port pairs (figure 3-5, column 4 lines 42-67, column 5 lines 1-18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the step as taught by Yoshifuji with the method as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 30**, and **as applied to claim 29 above**, Argentati discloses the claimed invention, but does not expressly disclose the method wherein the input port and desired output port pairs are grouped such that all pairs having the same entry switch matrix unit and exit switch matrix unit are grouped together.

In the same field of endeavor, Yoshifuji discloses the method wherein the input port and desired output port pairs are grouped such that all pairs having the same entry switch matrix unit and exit switch matrix unit are grouped together (figure 3, 4, 5, 8, column 5 lines 20-42, column 6 lines 34-58).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate grouping input and output port pairs as taught by Yoshifuji with the method as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 31**, and **as applied to claim 30 above**, Argentati discloses the claimed invention, but does not expressly disclose the method wherein the plurality of input port and desired output port pairs includes at least one input port that is to be connected to more than one output port.

In the same field of endeavor, Yoshifuji discloses the method wherein the plurality of input port and desired output port pairs includes at least one input port that is to be connected to more than one output port (figure 3, 4, 8, column 7 lines 5-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate at least one input port connected to more than one output port as taught by Yoshifuji with the method as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Consider **claim 32**, and **as applied to claim 31 above**, Argentati discloses the claimed invention, but does not expressly disclose the method wherein the input ports having the same entry switch matrix unit and multiple exit switch matrix units are grouped together.

In the same field of endeavor, Yoshifuji discloses the method wherein the input ports having the same entry switch matrix unit and multiple exit switch matrix units are grouped together (figure 3, 4, 5, 8, column 5 lines 20-42, column 6 lines 34-58).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate grouping input ports having the same entry switch matrix unit and multiple exit switch matrix units as taught by Yoshifuji with the method as disclosed by Argentati for the purpose of more efficiently mapping a CLOS switching network.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

a) Ayandeh (U.S. Patent # 6,914,902 B2)

b) Hu et al. (U.S. Patent # 6,653,929 B1)

c) Ma (U.S. Patent # 6,157,643)

d) Yoshifuji (U.S. Patent # 5,631,902)

e) Dally (U.S. Patent # 6,870,838 B2)

f) Swanson (U.S. Patent # 5,276,425)

16. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Suk Jin Kang whose telephone number is (571) 270-1771. The examiner can normally be reached on Monday - Friday 8:00-5:00 EST.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rafael Perez-Gutierrez can be reached on (571) 272-7915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Suk Jin Kang
S.J.K./sjk

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